Confidential A

MT7620A TFBGA PCB Layout Guide-V0.2

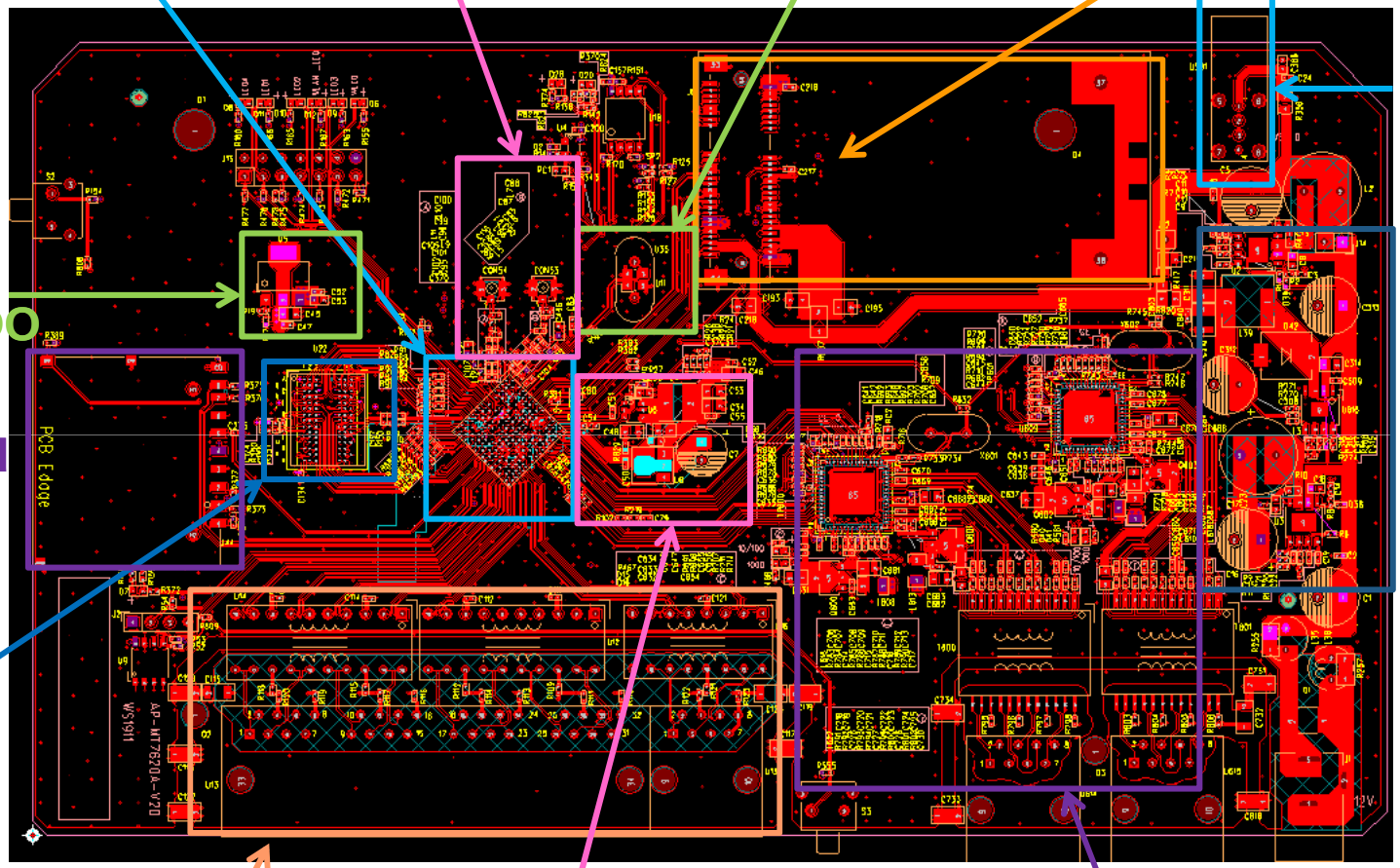
History

Version	Date	Description	Editor
V0.1	2012/07/05		Vedam/Kim
V0.2	2012/09/19	1. Update Power Plane 2. Change PA bias layout	Vedam/Kim
V0.3	2012/09/20	Update PCI-e maximum length	Kim

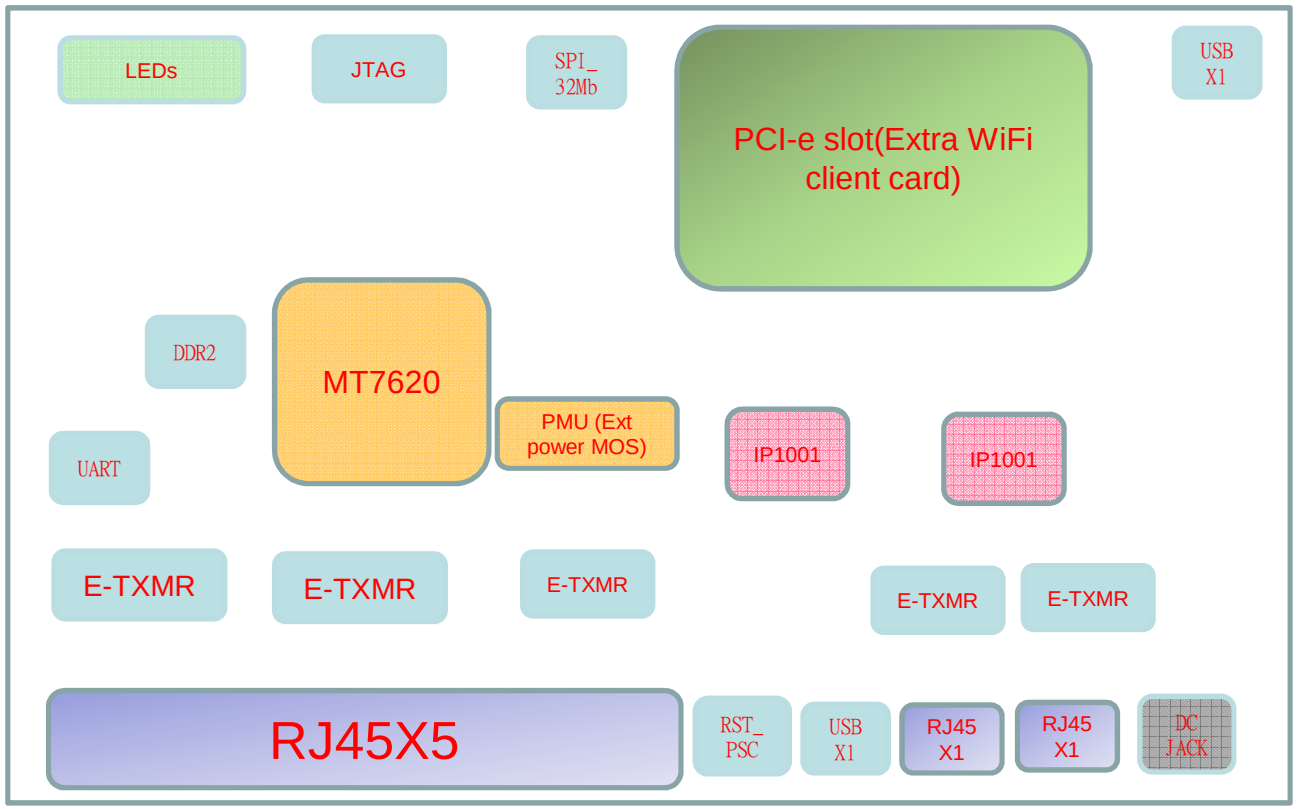
Content

- **MT7620A Layout design comment**
  - Placement
  - PCB Layer Stack
  - System Block Diagram
  - Power Topology
  - RF matching network
  - DDR2
  - PCI-e
  - Ethernet
  - RGMII
  - Others

Placement



MT7620A 11n 2X2 WiFi SOC_TFBGA 4FE+2GbE(or 5FE+1GbE) 4L PCB



Placement Comment

- Switching regulator and PMU circuit should be on lower right side of MT7620A.
- Ethernet port should be on lower left side of MT7620A.
- DDR2 should be on left side of MT7620A.
- 3.3V to 1.8V LDO should be close to DDR2.
- RF circuit should be on the top of MT7620A.
- Xtal should be close to MT7620, and clock trace should have ground plane around to avoid interference, but far away from RF circuit as possible.

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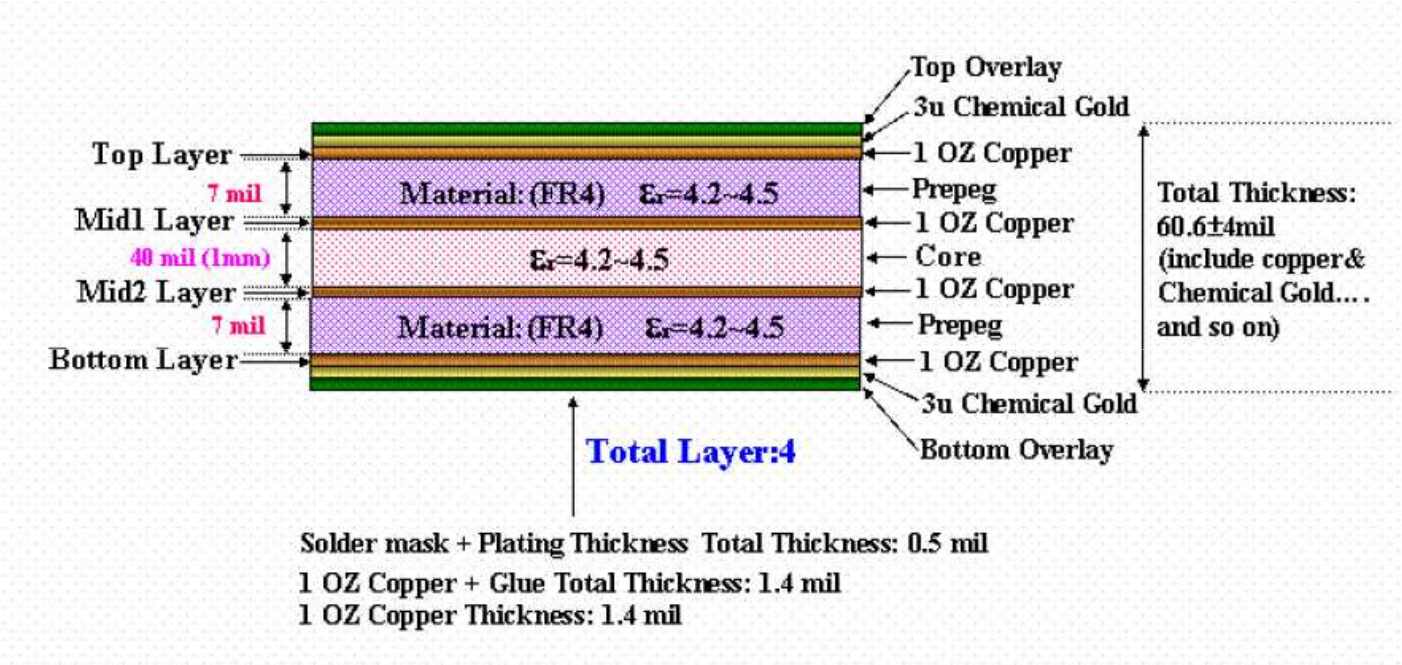
AP PCB Layer Stack (4 Layer)

Total Thickness:
60±4mil



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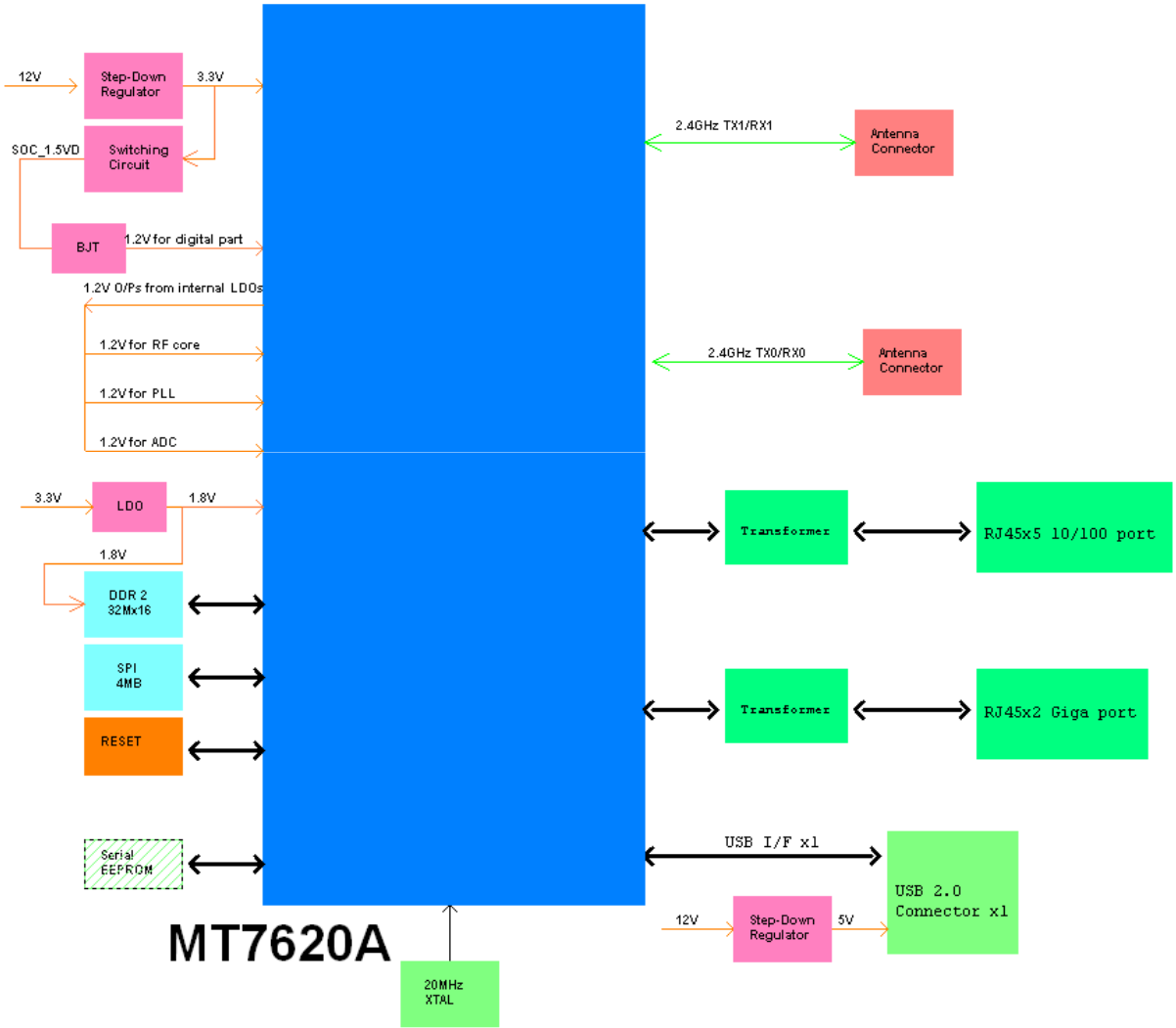
System Block Diagram



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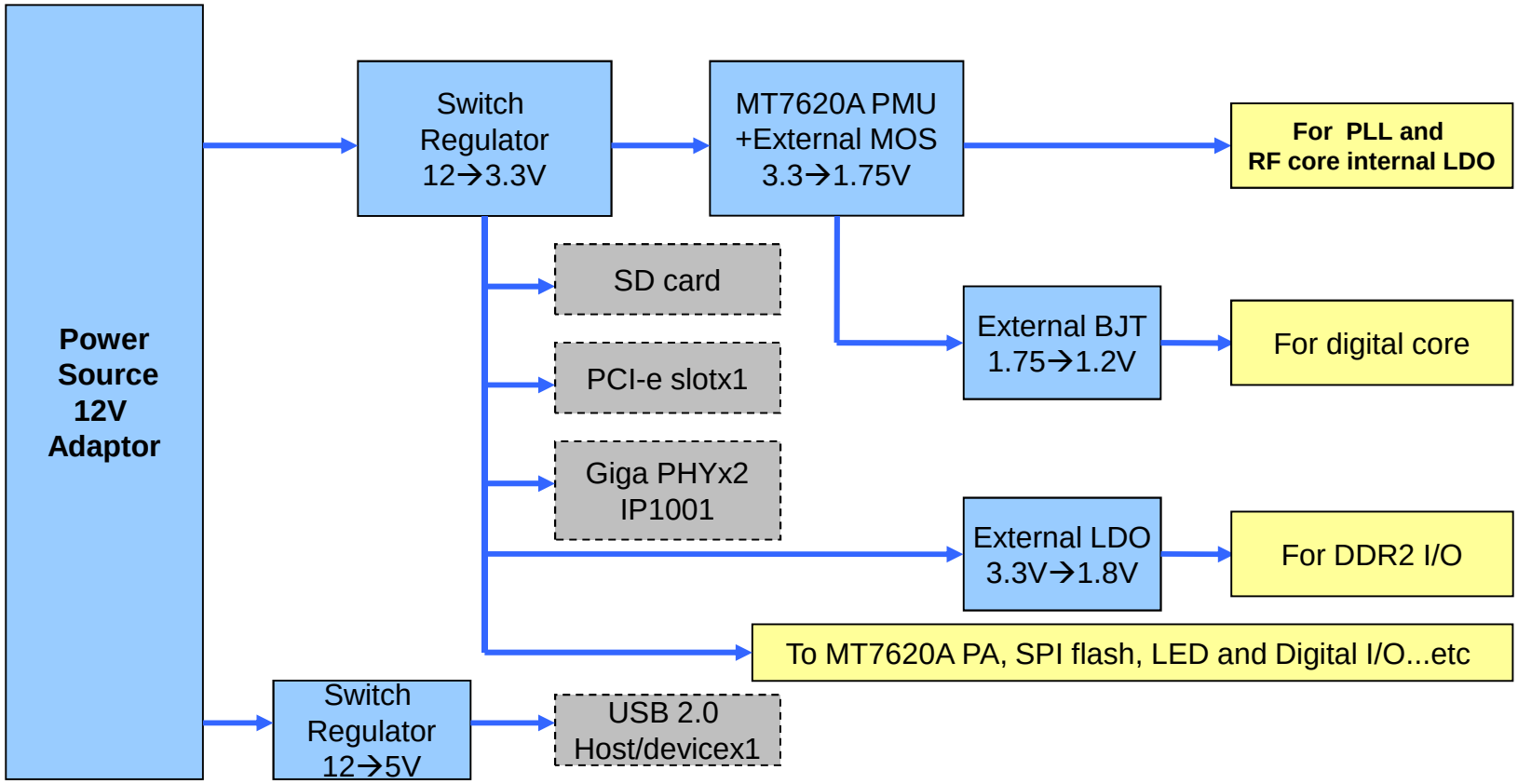
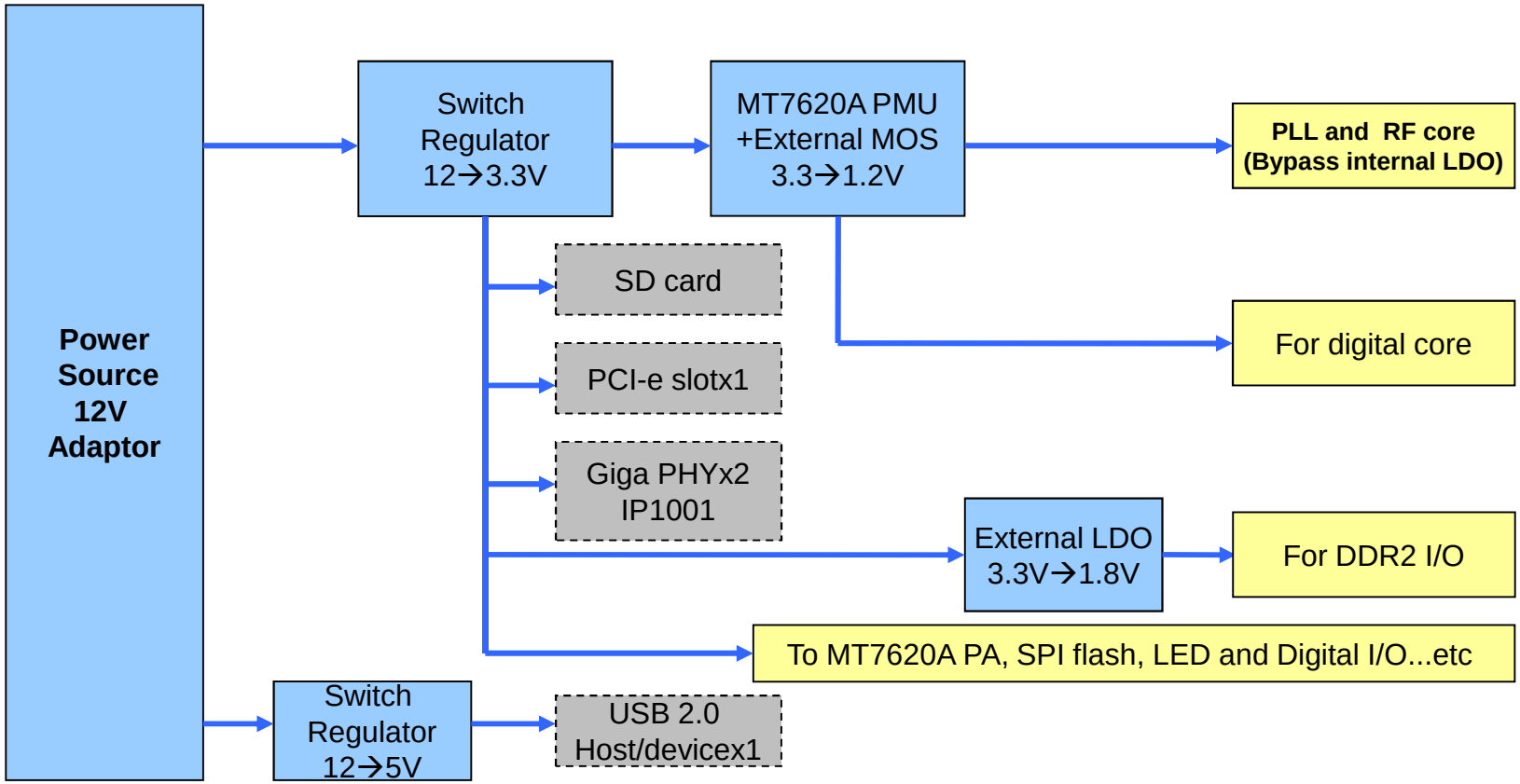
Power Topology



Power Topology(1.2V Optional)



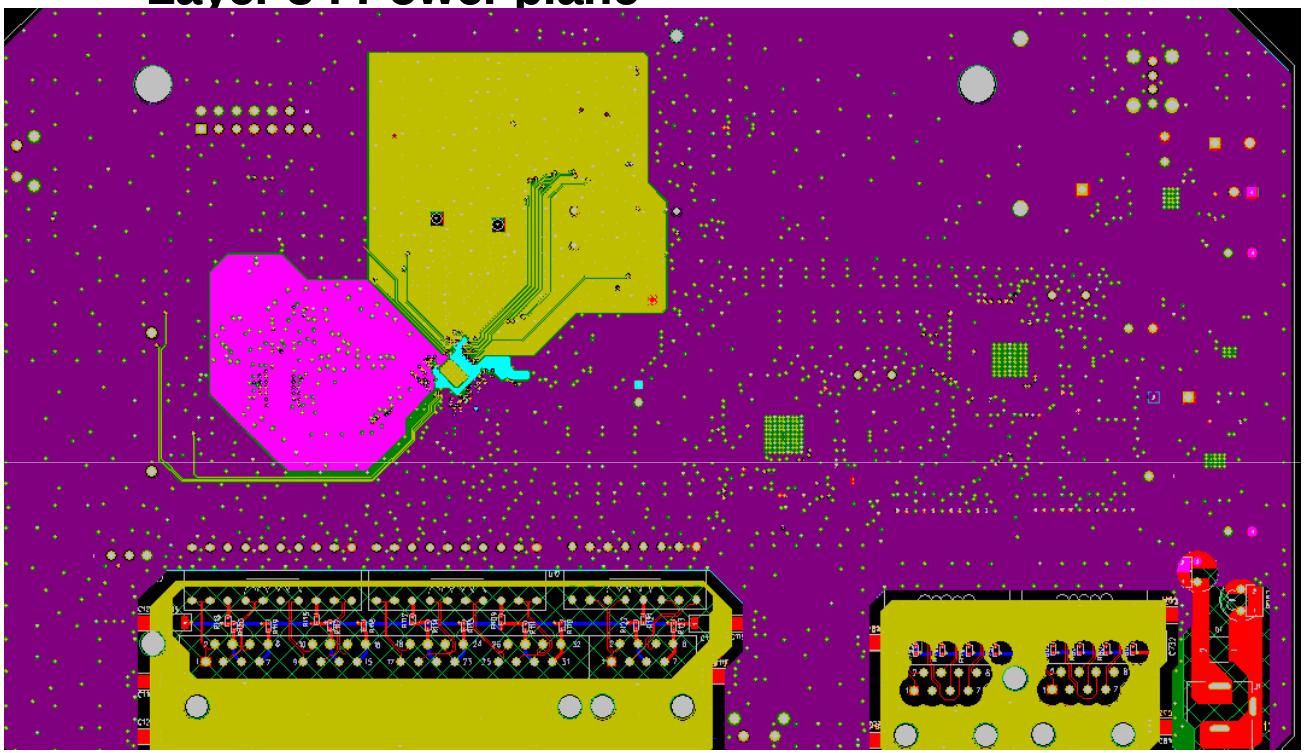
Power Consumption

MT7620A Main Power Pin and current

- RF part: PA2_V33N each pin 190mA
  PA1_V33A each pin 20mA
  VX_LDO each pin 25mA
- DDR2 part: DDRIO_V12D total 30mA
  DDRIO_V18D total 100mA
- EPHY part: EPHY_V12 total 58mA
  EPHY_V33 total 116mA

Power layout Comment

Layer 3 : Power plane



GND plane is for PA EMI issue

1. Don’t use 3.3V power plane for PA bias.
2. Hide those traces near PA in to layer 3.

- 3.3VD power plane
- DDR2 1.8V power plane
- DOC_1.25V power plane
- GND Plane

Power layout Comment

Bypass cap placement priority

- Of course, we hope every power pin has its own bypass cap and put cap close with.
- If can't, priority is as followed
  - RF Block:
    a. Soc_1.5VD for RF LDO.
    b. PA2_3.3V
    c. PA1_3.3V
  - Ethernet Block:
    a. SOC_V1.2VD
    b. 3.3VD
  - DDR2 Block:
    a. 1.8VD
    b. SOC_V1.2VD

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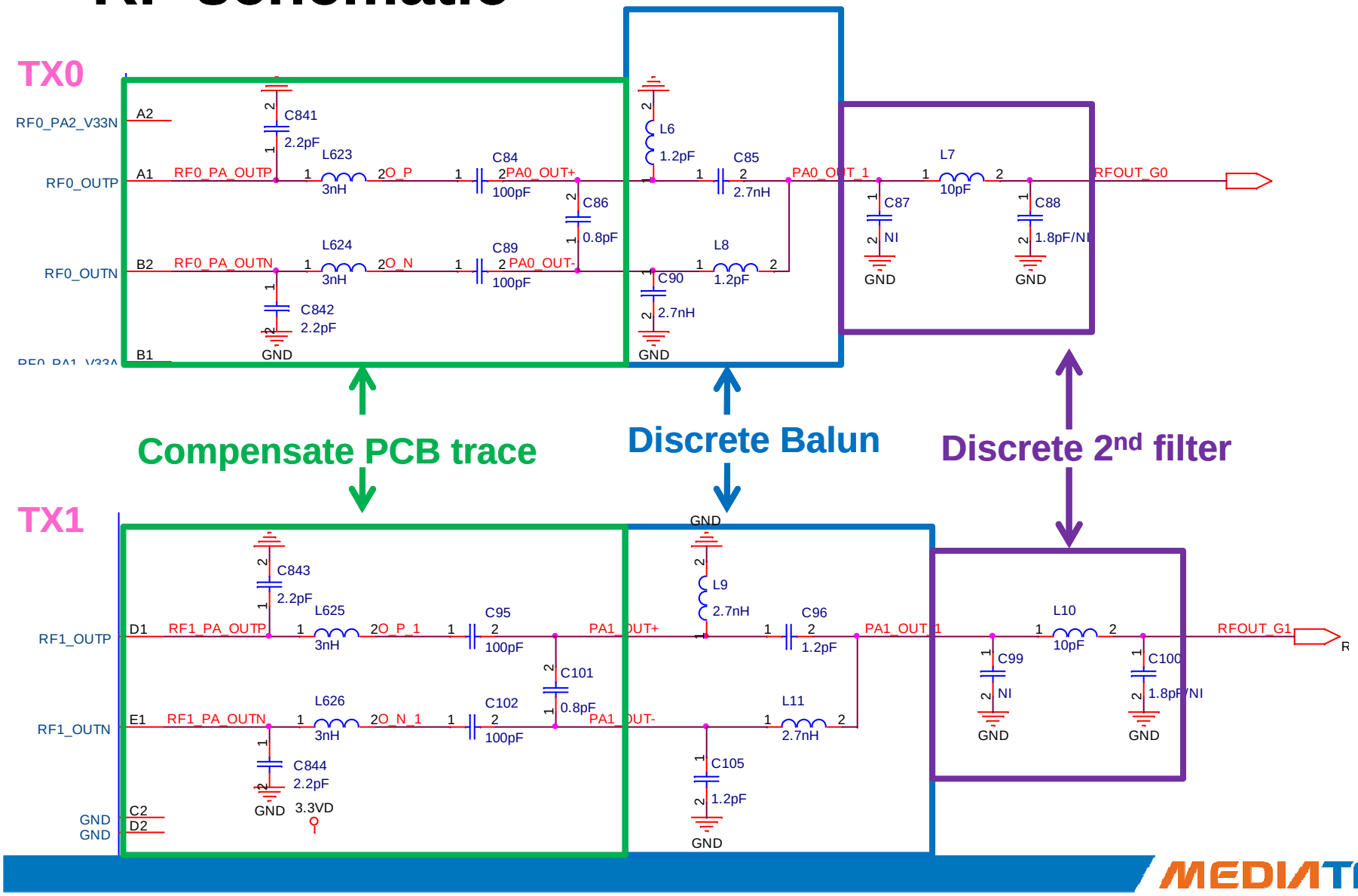
RF schematic



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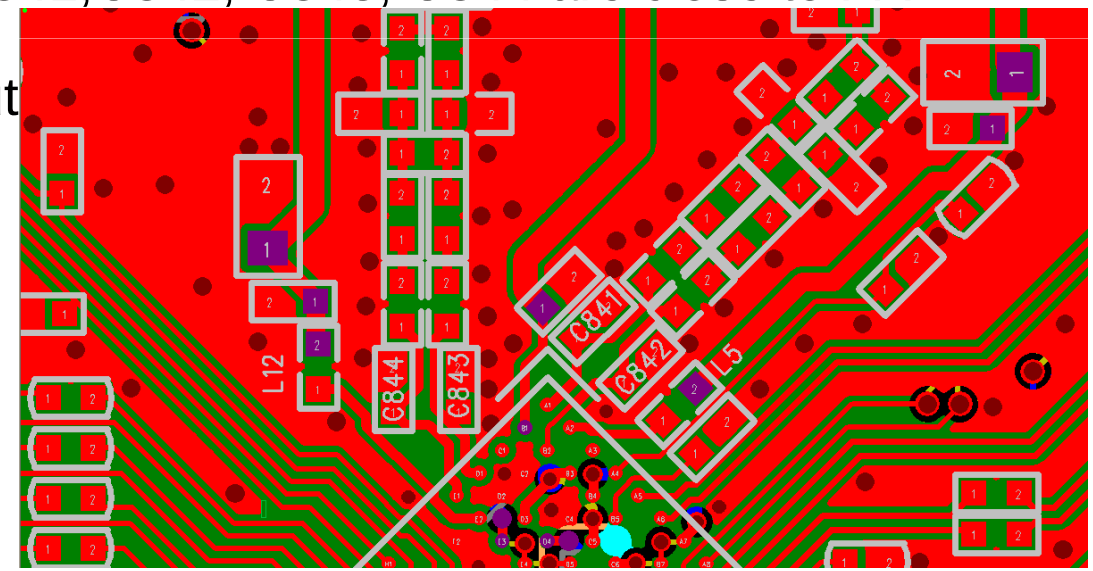
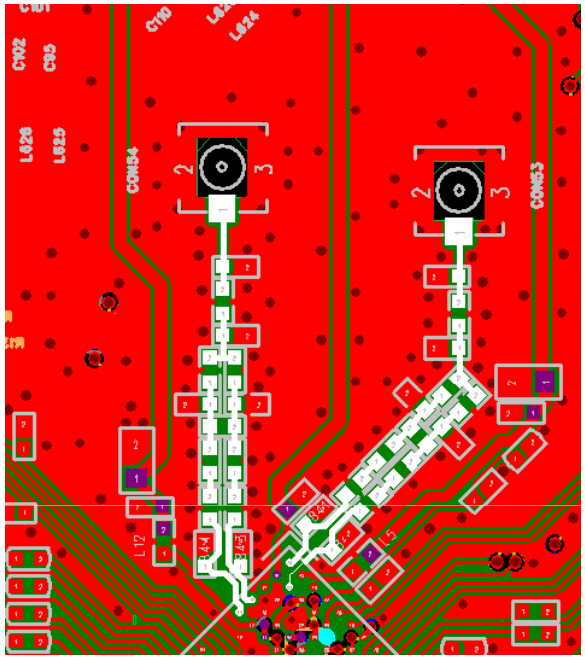
RF layout Comment

- It is strongly recommended to follow our reference layout exactly for the PA output matching and PA supply layout since that will impact output power, EVM and EMI.
- Ball A1,B2(D1,E1) is TX0(TX1) PA differential output, so its trace should be differential pair and equal length.
- Matching components C841,C842, C843, C844 are close to PA out as possible.
- For EMI issue, please put L12, L5 close to IC as possible.



RF layout Comment

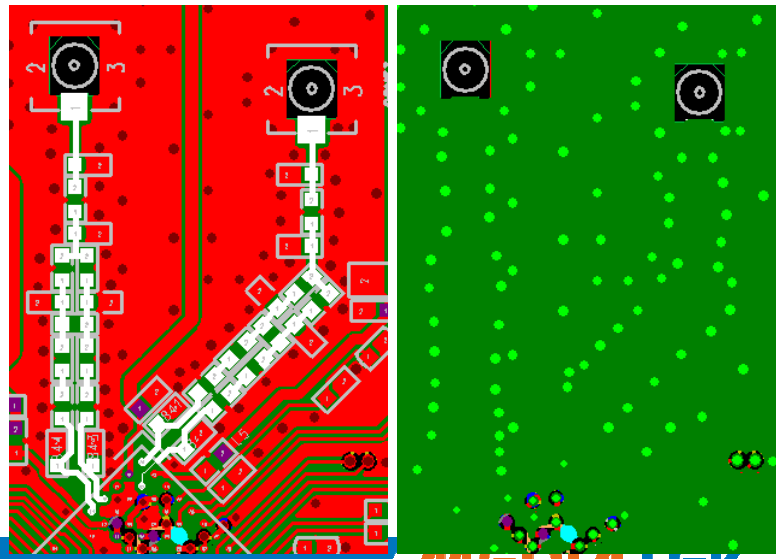


- Keep RF trace 50ohm impedance
- Trace width/space: 8mil/5mil

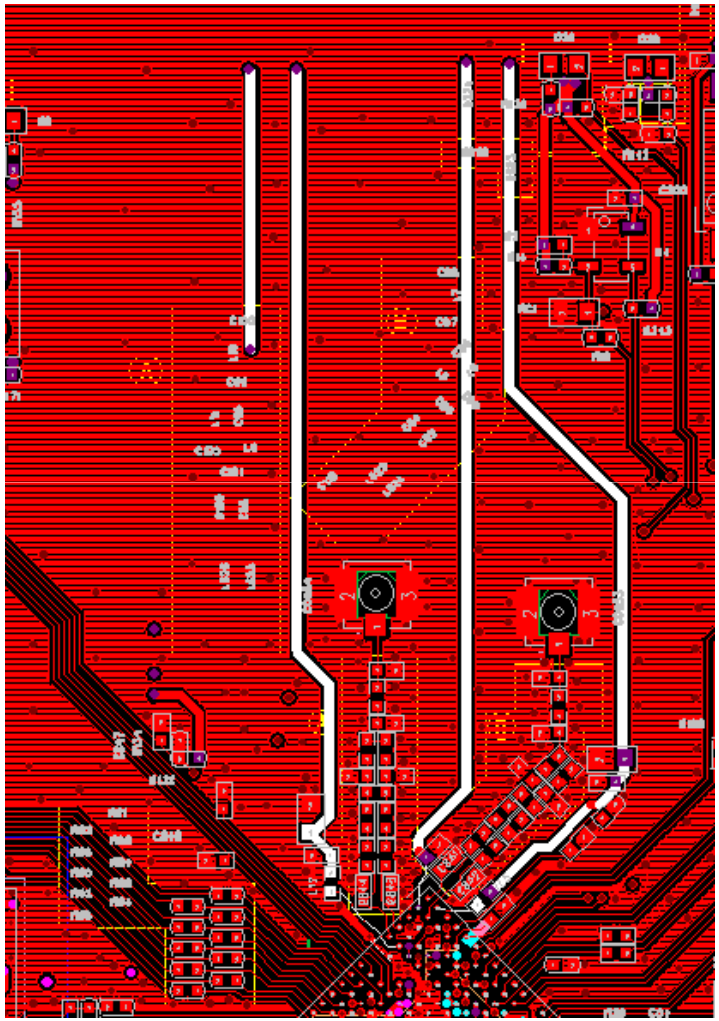
- Keep RF bottom layer as a perfect ground plane

Top layer

2nd layer

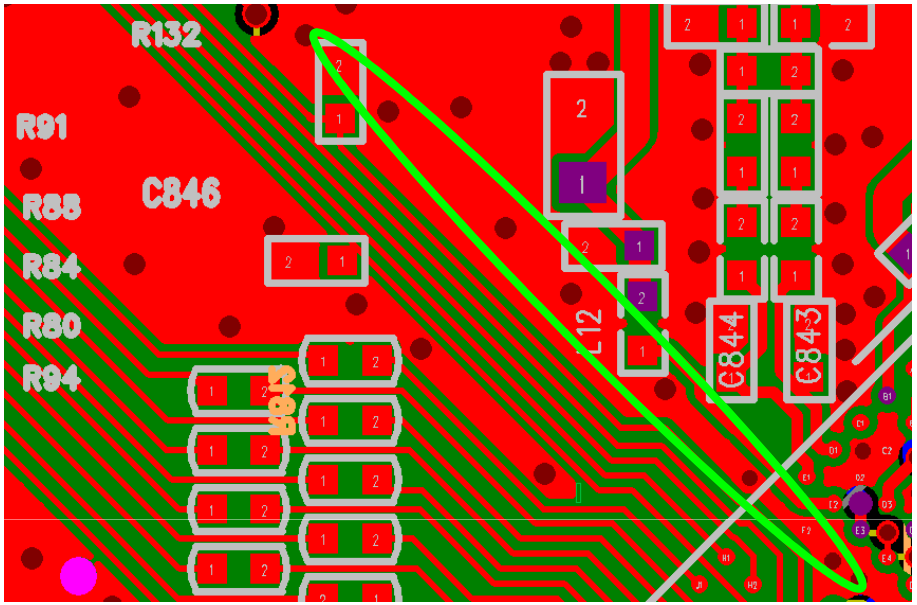


RF layout Comment



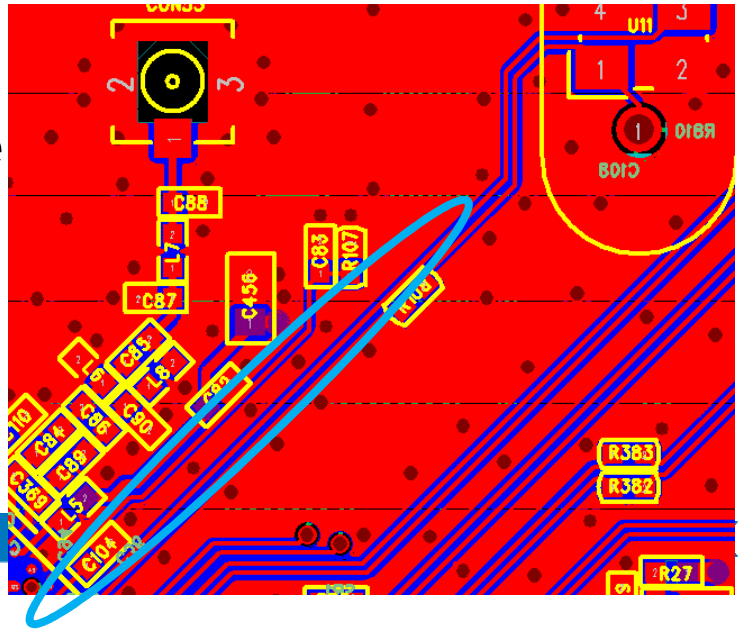
- Use power trace 3.3V for PA bias (Don’t use power plan)

RF layout Comment(Cont….)



- To avoid DDR de-sense, please add a GND wall between RF and DDR Parts like green circle

- To avoid crystal 20MHz de-sense, please add a GND wall between RF and crystal traces like blue circle



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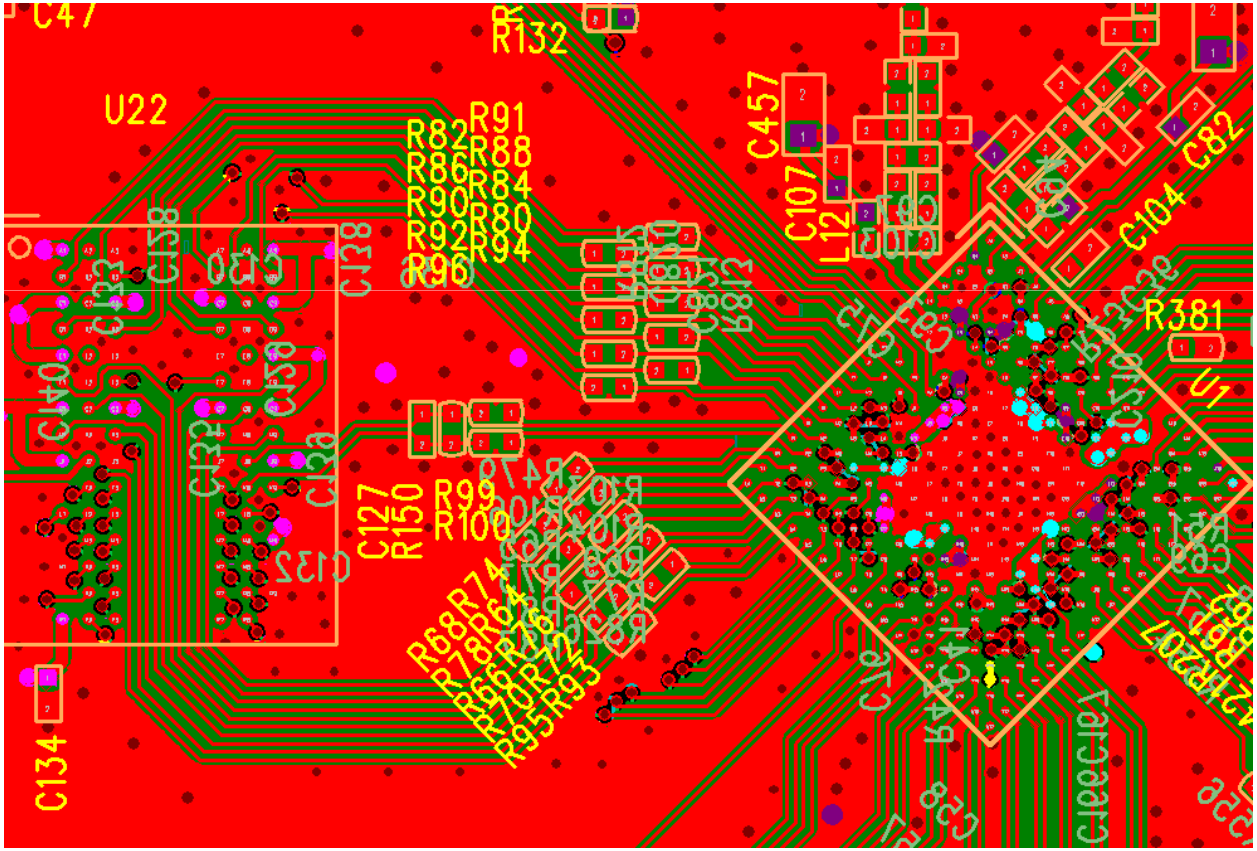
DDR2 Place

- Because Rx is very sensitive to noise floor, so it must be careful to place and deal with DDR2 power and data pin.



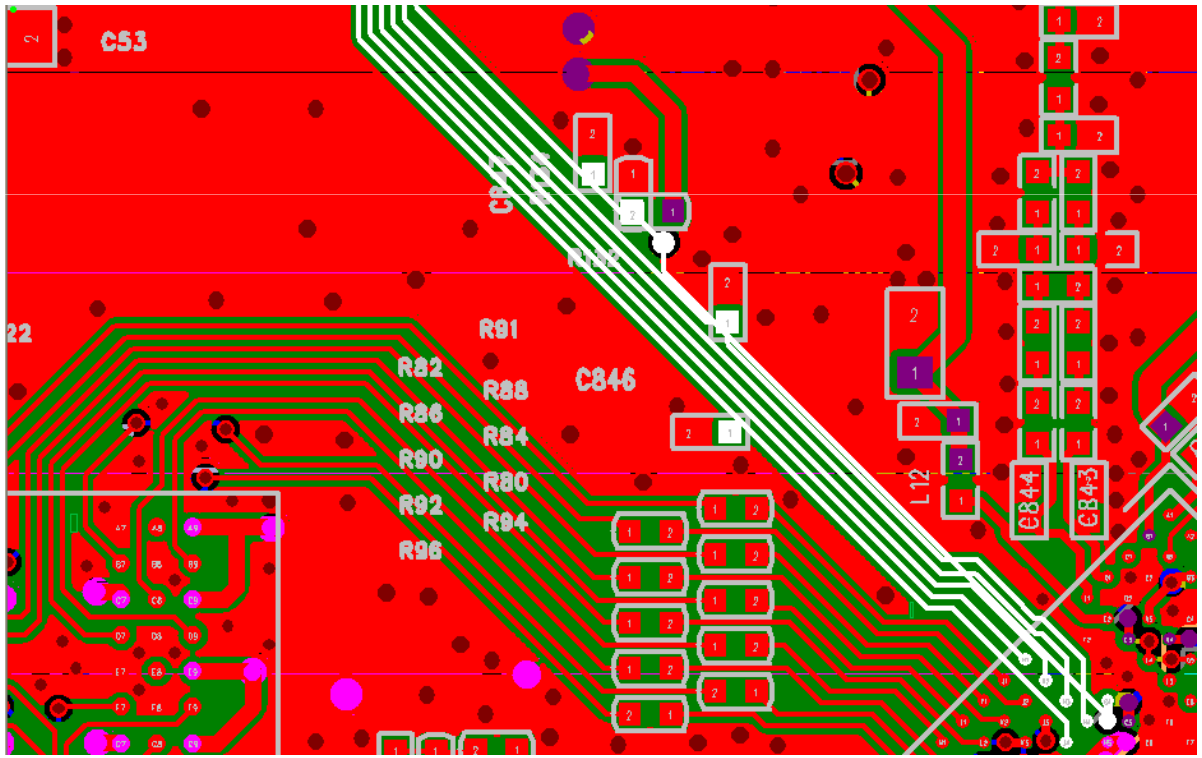
DDR2 PCB design guideline

- PCB adoption :
  - Adopt 4 layers or above PCB, that includes power and ground plane.
  - Consist trace impedance for single end signals
  - suggest impedance
    - single-ended = 50–60 Ω
    - differential = 100–120 Ω
- DDR2 signals group :
  - Clock group : CK
  - Data group : DQS, DQM, DQ.
  - Address, Command and Control group : Address (includes BA), Command (/RAS, /CAS, /WE), Control (/CS, CKE, ODT).
  - Power group : VDD/VDDQ, VREF.

DDR2 layout Comment

Isolation with RF

- Use LED trace to separate DDR/SDR ground with RF ground. That will make DDR/SDR and RF isolation better.
- Add de-caps on these traces to avoid DDR noise couple.



DDR2 layout Comment(Conti…)

Suggest routing

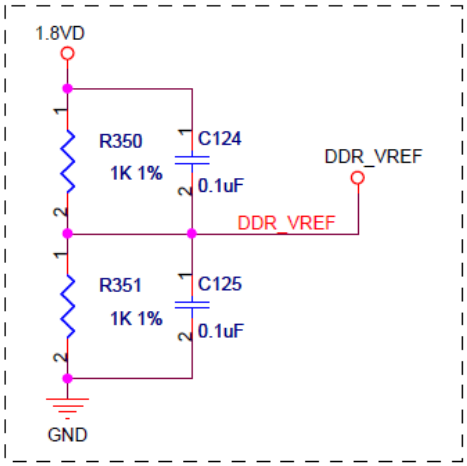
- Routing order: 1) Data, VREF, 2) Address/Command, 3) Control, 4) Clocks, and 5) Power
- Referenced to the solid ground plane.
- Place the series at the line for group signals with a 0~33Ω resistor.
- Layer transition should accompany GND via.
- DQ trace should be shorter than 1600mil.
- Reserve damping resistors and place these close to MT7620A
- DDR trace length control : DQ<->DQS: +/-100mil

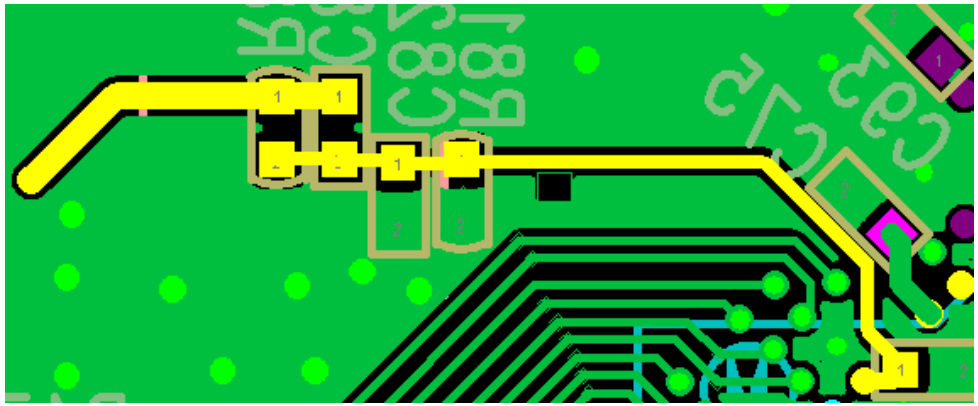
  CLK<-> DQS: +/-500mil

  CMD<-> CLK: +/-800mil

DDR2 layout Comment(Conti…)

- VREF should be wider and as short as possible, is isolated from noisy aggressor.
- Keep at least a 20–25 mil clearance from VREF and CLK to other traces. If possible, isolate VREF with adjacent ground traces.
- By using resistor divider network as VREF generator, make sure both resistors the same value and 1% tolerance.





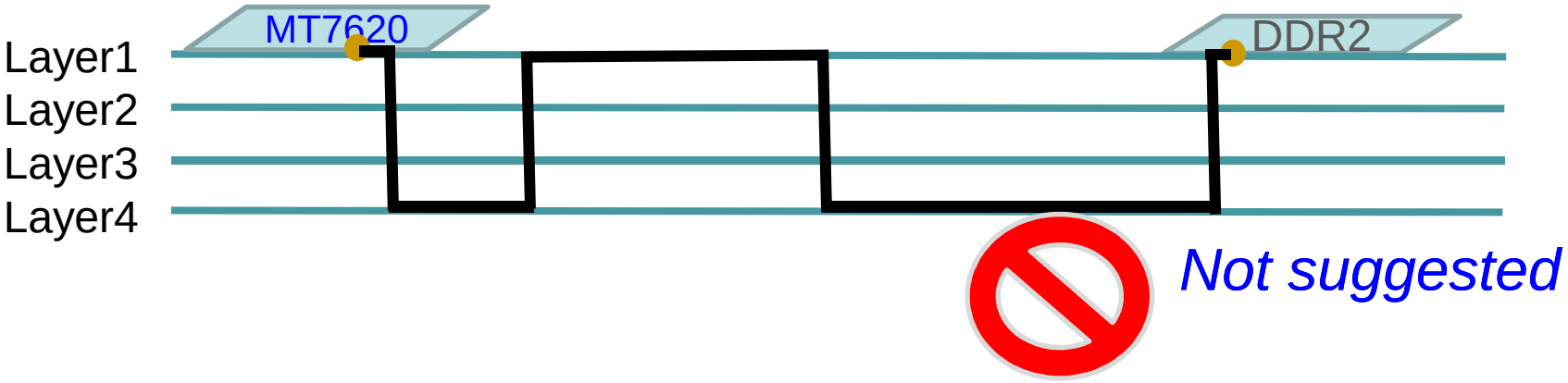
DDR2 layout Comment(Conti…)

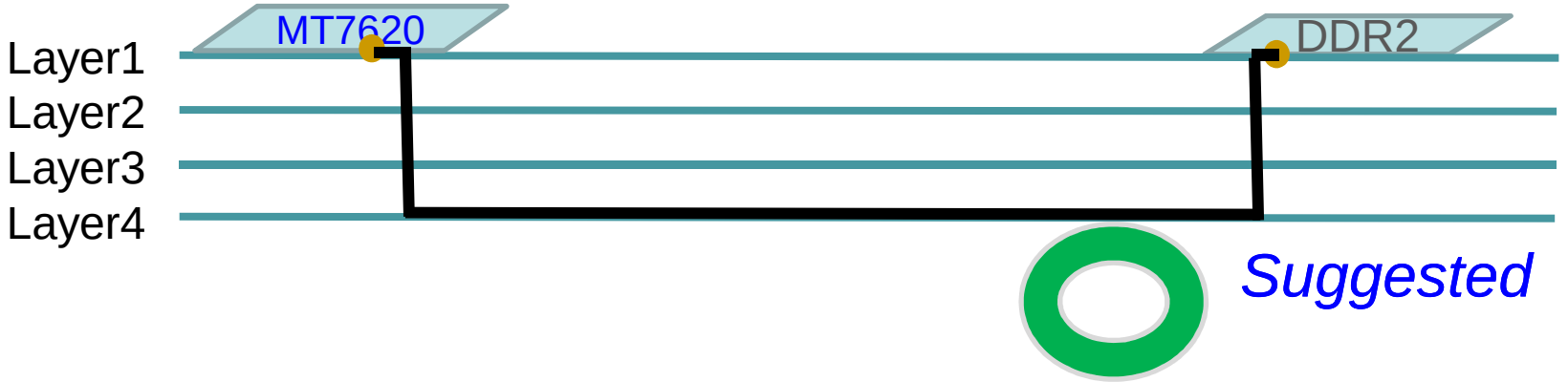
Suggest routing(Conti…)

- Reserve damping resistors and place these close to MT7620A

- If DDR used power routing: each trace should be wider than 12mil and we suggest Pin10 should have its own power trace, don’t share with other pins.

Reduce trace via





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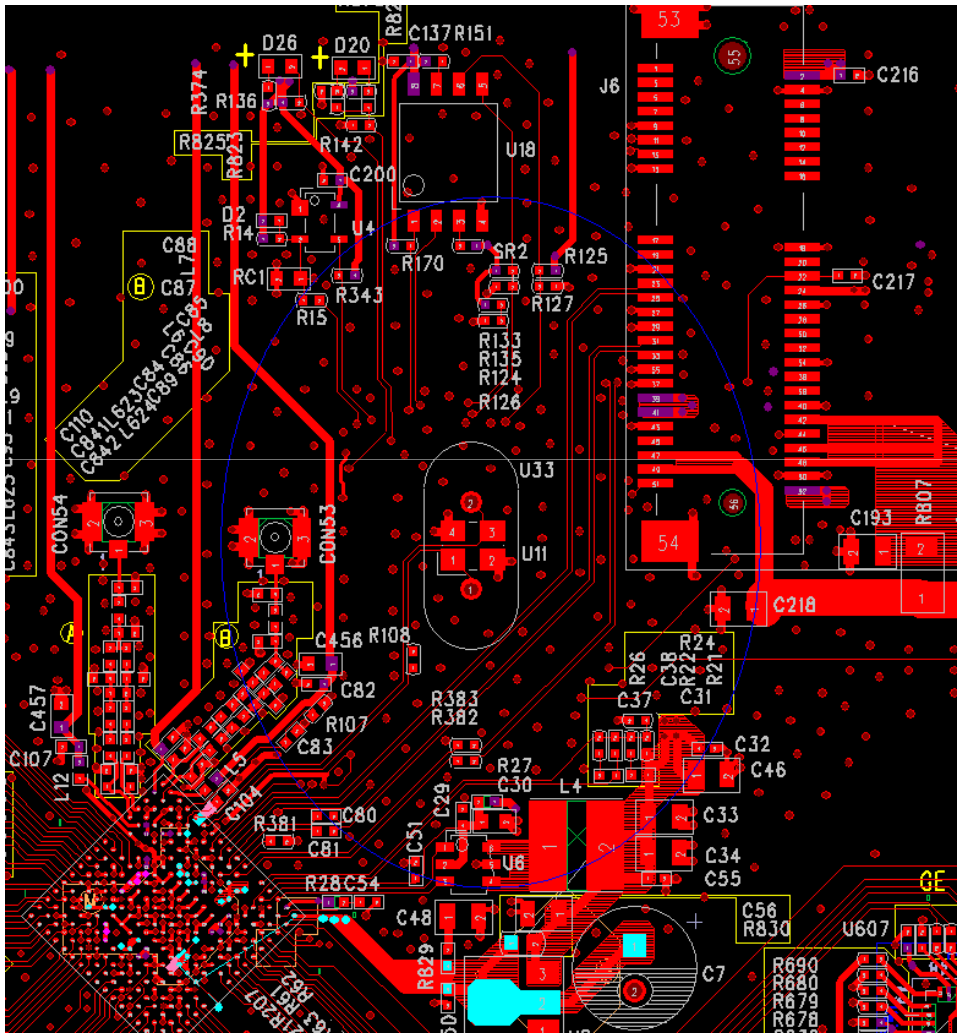
PCI-e

- Don’t over 5cm of all PCI-e trace length.
- Traces must maintain 100 Ω differential.



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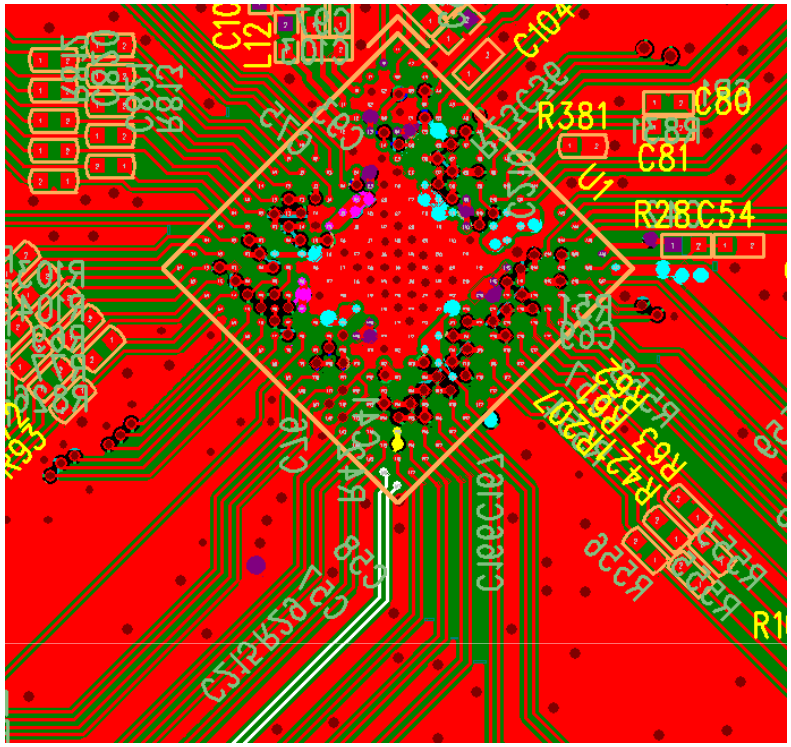
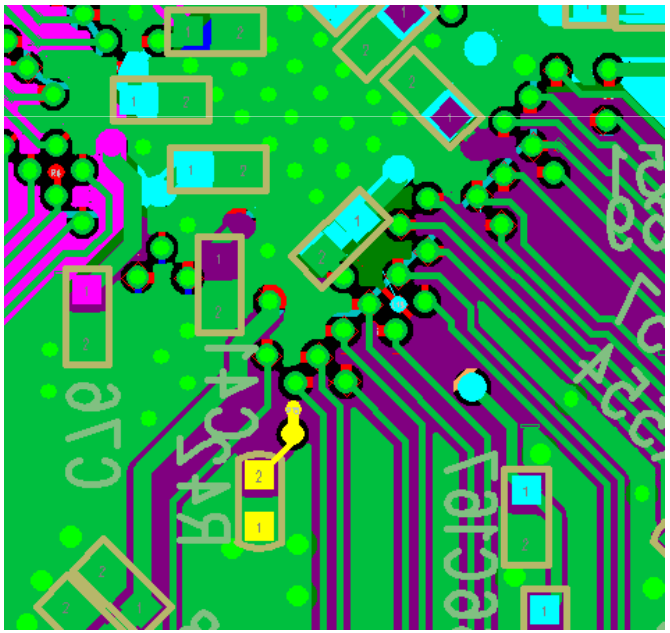
Ethernet

- Separate each EPHY pair with GND





- Put the EPHY_RES_VBG pin resistor close to SoC.

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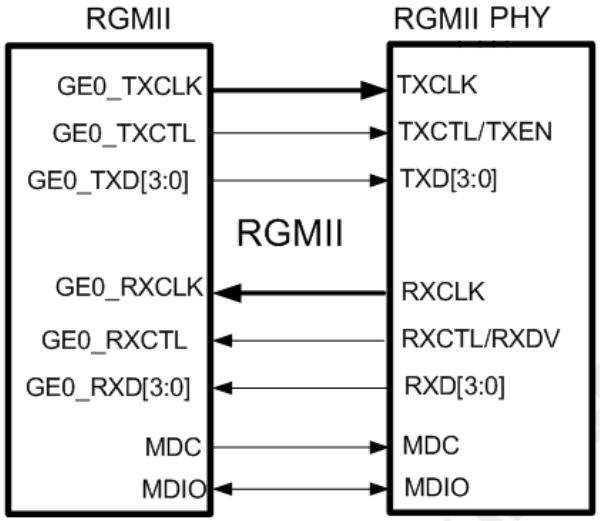
RGMII layout comment

- TXD[0..3]/TXCTL to TXCLK skew is as short as possible.
- TXD[0..3]/TXCTL internal separation needs 2 signal widths.
- TXD[0..3]/TXCTL to TXCLK cross- signal separation needs 3 signal widths.
- RXD[0..3]/RXCTL same TXD[0..3]/TXCTL layout comment.
- Keep RGMII TX signals trace routing in same PCB layer, also keep RGMII RX signals.
- Impedance is 50 ohm.



Content

- Package information and PCB Stack
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  - Power Plan
  - RF
  - DDR/SDR
  - PCI-e
  - Ethernet
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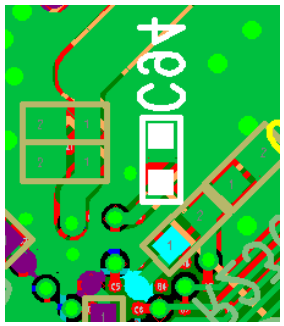
  - **Others**

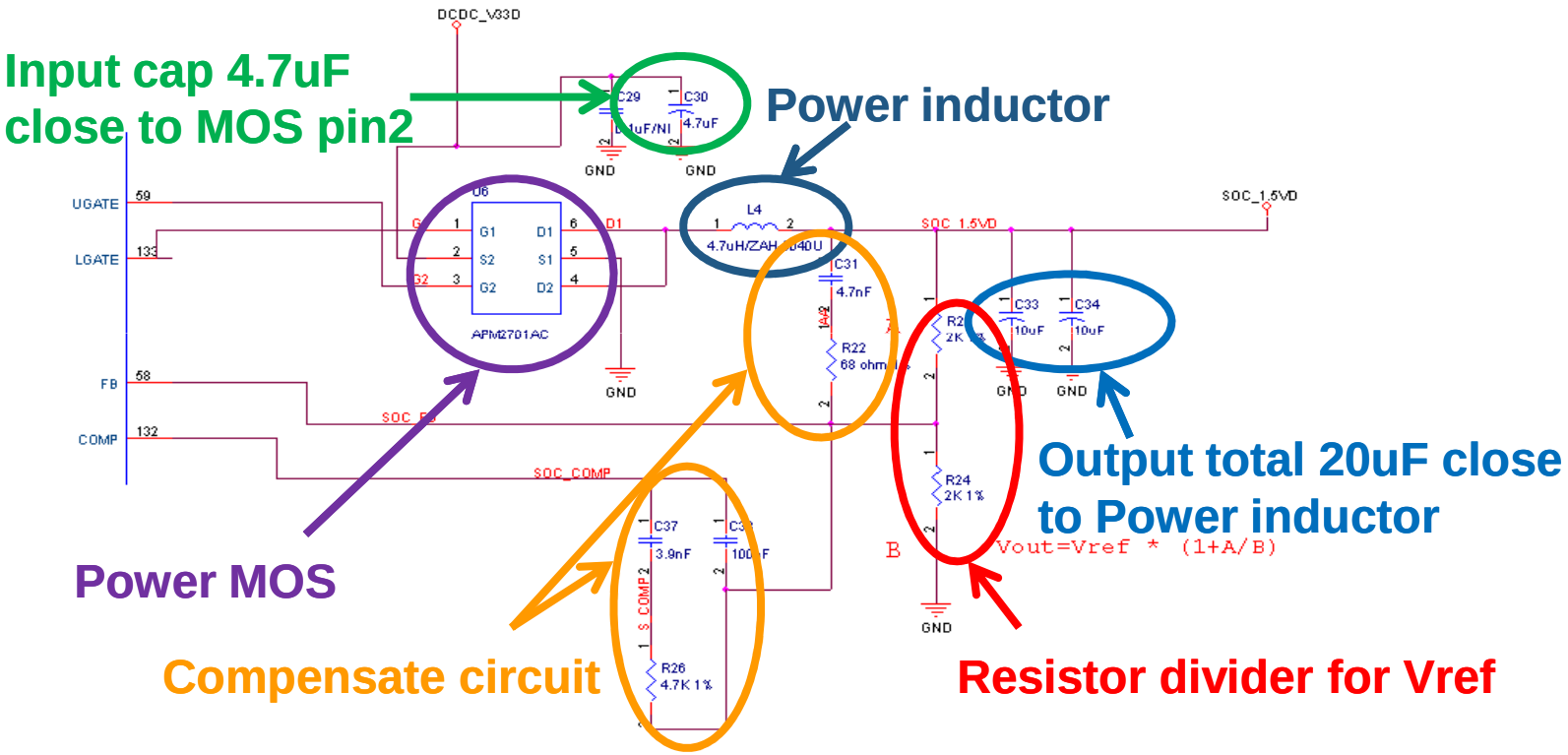
Others

- Antenna
  - It should be placed close to the RF connector and far away from noise source as can as possible.(like DDR, Xtal...).
- Frequency Reference Clock and Synthesizer Loop Filter
  - This The reference clock and synthesizer pins are sensitive to noise injection. Any noise injected to these pins will degrade the phase noise of the system. It is critical to place loop filter capacitor C94 as close as possible to ball B4(PLL_VC_CAP). C94's ground plane should be isolated from potential noise sources.



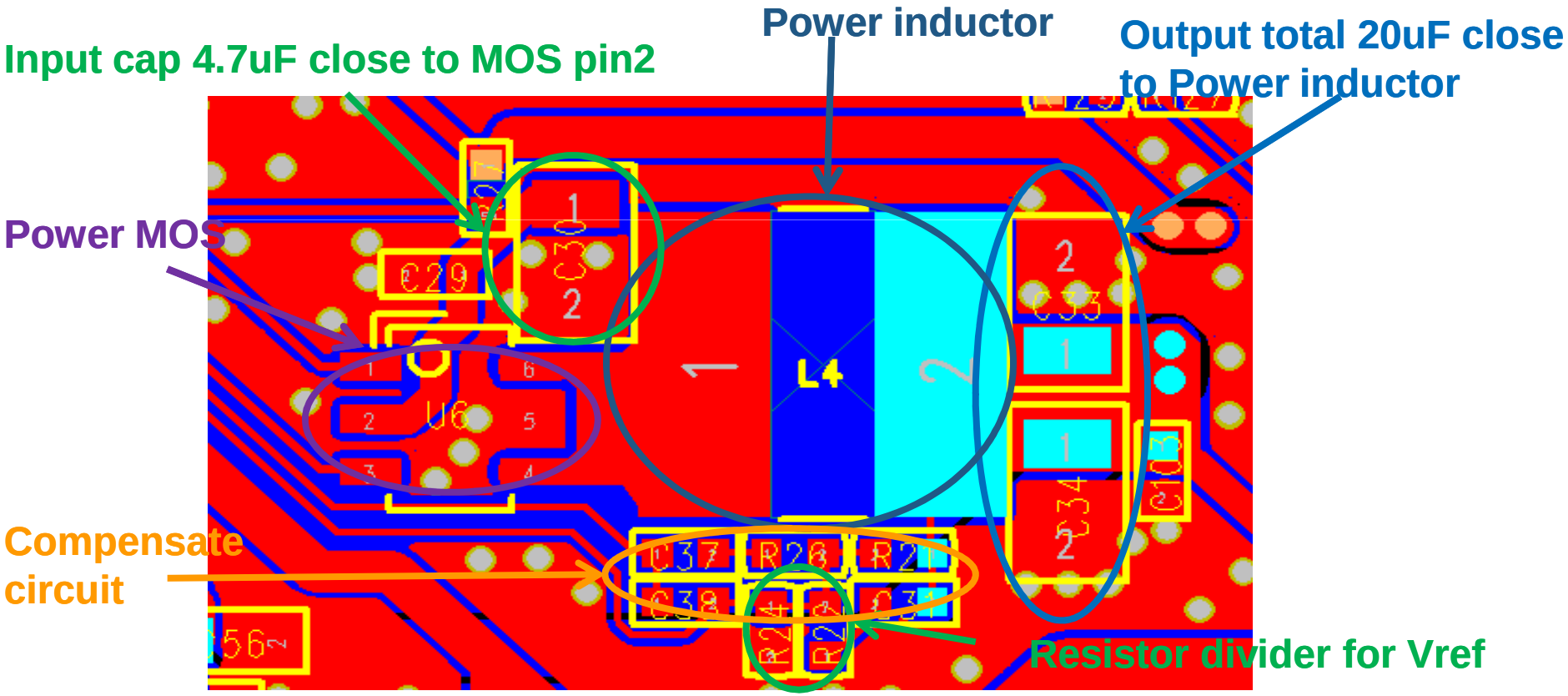
Others(Conti…)

- PMU 3.3V->1.75V switching Schematic



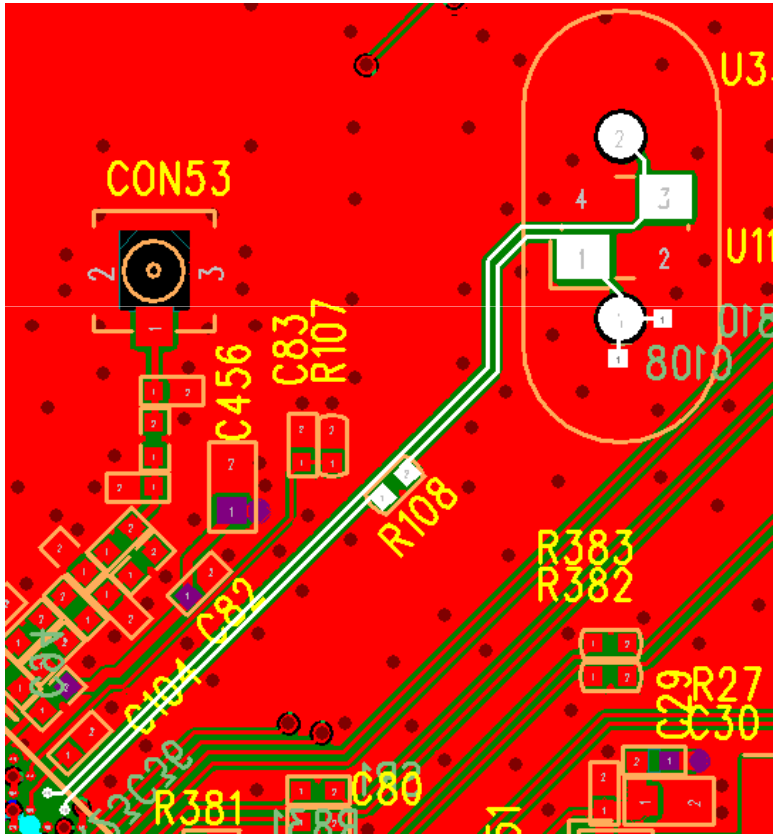
Others(Conti…)

- PMU 3.3V->1.75V switching layout
  Input power and Output power trace should be wider than 20mil.



Others(Conti…)

- Xtal Clock
  - Xtal clock trace should have ground plane around to avoid interference and keep at least 20mil from other trace.



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Q&A

Thank You !!

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